A 65-nm CMOS Implementation of Efficient PLL Using Self - Healing Prescalar

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Abstract: Nanometre scale technology introduces several issues in CMOS technology such as variability and leakage current that significantly affect the circuit performance. Devices performances plunge when variability is introduced inadvertently due to process variations causing device mismatching. Leakage currents are the main cause of malfunction of circuits at nano scale; they also degrade accuracy of analog circuits and make digital circuits to malfunction. Phase Lock Loops which are widely used in different application when made at 65nm technology face several functional and performance issues due to leakage currents which alter the states of digital systems and make analog systems less accurate. Calibrated Charge Pump, self healing prescalar self healing VCO are used in Phase locked loop to overcome above issues. In 65nm technology of CMOS with an active area of 0.0182 mm2 PLL is fabricated.

Keywords: Prescalar, VCO, PLL, CCP, TSPC

I. INTRODUCTION

As the dimensions of the device drop to nanometer scale levels, CMOS technology circuit performance is affected. This is mainly because the non-idealities of the devices have an upper hand in the operation of the devices which make them vulnerable to failures.

Malfunctioning of the devices is due to increase in leakage currents caused mainly due to plunge of the dimensions. The overall yield is reduced because of the variations in the manufacturing process. Malfunction affects analog and digital circuits. Digital circuits are affected by changes in their logic value at nodes affected by leakage currents, the parasitic capacitances along with the leakage currents either in charging mode or discharging mode is instrumental in altering the logic values leading to malfunction of the circuits.

Malfunctioning of the circuits is caused due to leakage in analog circuits which in turn affects accuracy and resolution. In nano scale technology, number of working devices on a wafer increases due to rise in temperature makes malfunction to become more severe. Therefore identifying the malfunction and automatically healing is achieved using additional circuitry in the device.

A control system called Phase Locked Loop accomplishes generation of output signal with its phase related to input signal. An electronic circuit consisting of a Variable frequency oscillator and a phase detector that compares the phase of the signal derived from the oscillator to an input signal is PLL. In a feedback loop oscillator is controlled by the phase detector. The phase of the input signal with the phase of a signal derived from its output oscillator is compared and phases are matched by adjusting frequency of its oscillator. Radio, telecommunications, computers and other electronic applications make use of PLL circuits.

Frequency is the derivative of phase. Input and output frequencies are maintained in lock state. Keeping the input and output phase in lock step implies frequencies of input and output are in lock step. Tracking of input frequency and a frequency is generated that is a multiple of input frequency is done by PLL. Indirect frequency synthesis is latter property and demodulation is former property.

To recover the signal from noisy communication channel stable frequencies are generated, or in digital logic designs, microprocessors clock timing pulses are distributed. Complete phase-locked-loop building block is provide by an IC, widely used technique in modern electronic devices, that exhibits output frequencies from a hertz to many giga hertzes.

Ring based voltage controlled oscillators common mode voltage is affected by phase locked loop leakage current and mismatching of device. Due to this Voltage controlled oscillator stops oscillating because its oscillating frequency range is affected. Between lowest and highest frequencies divider following a voltage oscillator should be operated in
wide range phase locked loops. Dynamic circuits are needed if a PLL working at a frequency at which the static circuits cannot work. For many phase locked loop designs True-single-phase-clocking dividers are commonly used. Over a wide range which includes temperature variations and deficiencies due to manufacturing, True Single Phase Clocking prescaler should be operated.

Original state of the floating nodes may be changed which limits the frequency range leading to malfunction because of unwanted leakage currents in TSPC prescaler. Reference spur and jitter will degrade due to current mismatches and presence of leakage currents in a charge pump.

II. LITERATURE SURVEY

The strong demand for low-power computing has been driven by a growing variety of portable and battery operated electronic devices. These span a broad range of performance and functions with respect to throughput. Power consumption is a limiting factor in VLSI integration for portable applications. As the supply voltage scales down with the technology, any power supply noise on power and ground level affects the analog circuit performance more than before. This power supply noise has a direct effect on the Voltage Controller Oscillator (VCO) output frequency of PLL which is proportional to the control voltage from the charge pump. Therefore, this power supply noise is a critical issue to be resolved for better jitter performance of PLL. In addition, due to the continued scaling of technology, leakage power has become dominant in power dissipation of nano scale CMOS digital circuits [3]. Since the analog electronics has to be on the same die as the digital core in contemporary mixed signal circuits, it has to cope with the nano scale CMOS issues. Nano scale CMOS technology has come to a point where new phenomena need to be taken into account for analog circuits. Threshold voltage decreases and gate oxide becomes thin as the nano scale process enhances. The significant issue in CMOS circuit design is leakage current nano scale process.

Gate-source voltage (Vgs) and drain-source voltage (Vds) will affect CMOS current in nano scale CMOS process, since the leakage current (Vgs<VT, Cut-off MOS) is affected by drain-source voltage (Vds). This makes the cascode current sink/source topology more desirable for the current mirror circuit in low power nanoscale circuit design.

The leakage current increases with the transistor size of CMOS and the VCO output frequency is more sensitive to the leakage current and its control voltage (VC) in high frequency operation.

Therefore, for large multiplication factor in PLL, the leakage current has a considerable effect on the control voltage (VC) variation of the VCO after the large feedback cycle detection. Consequently, the leakage current is an important issue to be addressed for the PLL jitter performance.

III. PROPOSED ARCHITECTURE

The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. Divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units that is used by dual modulus prescaler. Divide-by-2/3 unit operation at the highest input frequency of the prescaler design makes it the bottleneck. D flip-flops (DFFs) and additional logic gates are used for obtaining different division ratios, which introduces additional program delay to reduce operating frequency.

The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components. In modern wireless communication systems, the power consumption is a key consideration for the longer battery life. The MOS current mode logic (MCML) circuit, which is of high power consumption, is commonly used to achieve the high operating frequency, while a true single-phase clock (TSPC) dynamic circuit, which only consumes power during switching, has a lower operating frequency.

The conventional divide-by-4/5 dual-modulus prescaler using TSPC DFFs is shown in Figure.1(a), the nodes under observations are A and B in the TPSC shown in the diagram, the logic states at nodes A and B can get altered due to leakage currents which are undesirable. Malfunctions at nodes occur due to leakage currents through the parasitic capacitances associated with a node and ground. A leakage current discharges it to ground and the other case is when node A is low and a leakage happens to the supply through the parasitic capacitance which makes the node A to high which is not the desired state.

At the node B in figure.1, if the leakage current makes the node to go high when clock is it does not affect node B, therefore we are not considering node B here.

Occurring of malfunction at the node is shown in simplified circuit of Figure.1 (b). Assuming that the transistor M1 is turned off with low clock. The leakage current through M1 is more than M2 and M3,because a low leakage current is induced into cascade transistors, M2 and M3.
To study the effect of a malfunction at a node let us look at the schematic circuit given at Figure 1(c). To start with let us take the initial condition, that the transistor M1 is off, when the CK is low, the starting state of the node is low. As the node is not tied to logic high or low, due to a malfunction the node may get charged through M1 by means of a leakage current and the node will become high. The leakage current through M1 is greater than that of M2 and M3, this is because of the cascade connection of transistors M2 and M3.

The pulse generator creates a short pulse at the gate of M2A transistor, when the Clock signal becomes high, this will clear. On the rising edge of the clock CK and when the D input is high, the output of the D flip flop Q to go high, which will turn off the transistor M3A. The pulse generator connected to M1A outputs a low pulse at the gate of M1A, which will make the M4A to turn OFF.

Due to the undesired leakage current, it is assumed that Q is charged high, before the arrival of the next clock pulse. Next Q goes low to make M3A to ON condition and makes Dlk high. Dlk going high is the indication that a malfunction has occurred in the TSPC D flip flop. The ratio of areas of M4A and M3A is 5 to make sure that M4A and M3A are turned on. Simulation and verification for all corners were done for a supply variation of 10% and with the temperature in the range of 0 to 100 degree centigrade. The timing diagram is shown in the right-hand side of Figure 2(b) when the malfunction is fixed.

With respect to Figure 2 (a) when Enable signal goes high, it implies that a malfunction has occurred and that information is latched and the compensator is made active. To start with let us assume that the initial state of Q bar is low and that the node is getting charged by the leakage current. The transistors, M5A–M8A, in the compensator will turn ON since

Figure 1 (a) prescaler using TSPC DFFs. (b) At a two kinds of malfunctions are occurred. (c) At Q bar the malfunction.

Healing this fault is accomplished with the help of a self healing circuit; the proposed circuit is shown in 2(a). This circuit consists of three compensators and one detector. The timing diagrams of the self healing circuit without and with a malfunction are given in figure 2(b). The operation of the circuit can be described as follows, let us assume that the Enable signal is low to start with, this will disable the latch in fig 2(a) . In case a malfunction is detected, the circuit will operate as given in the timing diagram in figure 2(b).
Q bar is low. A Transistor M7A with a small area is chosen to counteract the leakage current. Simulation and verification for all corners and a supply voltage variation of 10% at the temperature of to 100 degree centigrade were done. In a similar manner repair of the state at the node A will be done when a malfunction is detected, this will be done through M7B or M7C to counteract the leakage current.

IV. SIMULATION RESULTS

Figure 3 Phase Locked Loop

A digital-controlled CP, 4-bit encoder, self healing VCO, programmable divider, time-to-digital converter (TDC), Phase - frequency detector (PFD), lock detector (LD), and 2nd order passive loop filter are present in PLL. A 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler is present in programmable divider. The division ratio is from 4 to 131.

Figure 4 4-bit digitally-controlled charge pump.

4-bit digitally-controlled CP determines amount of current mismatching. Charge pump realigning is done through TDs digital code. The power attained when the simulation of the TDC was done was 0.24 mW. The dynamic range is 4.8 ns and the time resolution is 0.3 ns. Figure 2.5 shows a 4-bit digitally-controlled CP. The down current is digitally controlled within 180 and 210 micro Amperes; up current has a nominal value of 200 micro Amperes. An operational amplifier with high gain and stability is required for the traditional replica-biased CP. Static power will be consumed by this operational amplifier. Due to digital calibration CP calibration can be done quickly. After the calibration is done, the digital code is fixed and TDC is shut down to save power.
Finally, we have presented information on developing a wide-range PLL in a 65-nm CMOS process, the methodology adopted here is to identify the current leakage at a node and then to develop analog and digital circuits which can counteract the affect of these leakages. A PLL was developed with self-healing prescaler, a self-healing VCO, and a calibrated CP. In future self healing prescaler can be implemented in 45-nm technology to increase the accuracy.

**REFERENCES**


