D.C and A.C Analysis of Common Source Amplifier with Resistive Load Connected Using Cadence Virtuoso

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Abstract: In this paper we are going to discuss about the common source amplifier with resistive load connected and the implementation of the CS amplifier with resistive load connected in the cadence virtuoso tool and checking the output results of D.C analysis, A.C analysis, Transient analysis and finally designing the layout of the CS amplifier with resistive load connected using cadence virtuoso 180nm Technology.

Keywords: Common source Amplifier, Resistive load, D.C analysis, A.C analysis

I. INTRODUCTION

Amplifiers are the basic building blocks for both digital and analog systems. To amplify the weak signal we are using the amplifiers for further processing, the effects of noise in the next stage is also reduced and give the logic levels properly. In the feedback systems, amplifiers play an important role [1]. The single stage amplifiers are basically three types.

1. Common Source
2. Common drain
3. Common gate

1. Common Source:

In common-source amplifiers, the input is connected to the gate and the output is taken from the drain. We can divide common source amplifiers into two types, one is without source degeneration and another is with source degeneration [1][2][3]. The block diagram of common source amplifier is given in figure 1.

![Figure 1: Common Source Amplifier](image1)

Figure 2: Common-Drain Amplifier

2. Common Drain:

The common drain amplifier is also called as a source follower and it can be used as a voltage buffer. In this type amplifier, the gate terminal of the transistor gives input and source give output and drain are common to both input and output [1]. The block diagram of common drain amplifier is given in figure 2.

![Figure 2: Common-Drain Amplifier](image2)

3. Common Gate:

The common gate amplifier can be used as a current buffer. In this type amplifier, the source terminal of the transistor gives input and drain give output and gate terminal is common to both input and output [1]. The block diagram of common gate amplifier is given in figure 3.

![Figure 3: Common-Gate Amplifier](image3)
1. Resistive Load
2. Diode-connected Load
3. Current Source Load
4. Triode Load

The following parameters of amplifiers are very important:
- Small-signal gain
- Voltage swing

1. Resistive Load:

In this type, we use the resistor as load

- The region operation of M1 depends on its size and the values of Vin and R.[5]
- There are two methods to calculate the gain.
  1. Small-signal model
  2. Large-signal analysis [1]

1. Small Signal model:

The small signal model for common source amplifier is given in figure 4.

![Small Signal model for Common Source Amplifier](image)

In this we assuming that the transistor is in the saturation region, and channel length modulation is ignored.

- The current through RD: \( i_D = g_m V_{in} \)
- Output Voltage: \( v_{out} = -i_d R_D = -g_m V_{in} R_D \)
- Small-signal Gain: \( A_v = \frac{V_{out}}{V_{in}} = -g_m R_D \)

To increase the gain:

II. IMPLEMENTATION

In this, we are implementing the CS amplifier with a resistive load connected. We have designed this by using the Cadence virtuoso in 180nm technology and performed the different types of analysis and designed the Layout of the CS amplifier with a resistive load connected.[4].

1) D.C analysis of CS amplifier with resistive load connected:

The design of the D.C analysis of CS amplifier with a resistive load connected is done and the D.C analysis output wave form of the CS amplifier with a resistive load connected has been obtained.

i) Schematic of D.C analysis of CS amplifier with resistive load connected Design steps:

1. From the cadence window selects the FILE→LIBRARY to create the new library and attach the library to the existing library.
2. To design the schematic go to the FILE→CELL VIEW and attach to the library and name the cell and press ENTER
3. The Schematic Editor window will be open where we can design the required NMOS design.
4. To get the NMOS symbol press (I) the instances window will be open then select gpdk180→NMOS→Symbol.
5. To get the PMOS symbol press (I) the instances window will be open then select gpdk180→PMOS→Symbol.
6. Select the input ports and the output ports select port (P).
7. For D.C analysis, the input is given as the VDC and the voltage is given as the 0.75V to bring both the transistor in the saturation region. The schematic of D.C analysis is shown in figure 5.

![Figure 5: Schematic of D.C analysis](image)
The output waveforms of the common source amplifier with a resistive load using D.C analysis is given in figure 6.

2) A.C analysis of CS amplifier with resistive load:

The schematic design for the A.C analysis and the D.C analysis is same but the only one change is that the instead of the VDC we give the $V_{\text{sin}}$ for the input. The schematic is shown in figure 7.

Design Steps for Layout:
1. Now to design a layout some modifications must be done in the schematic.
2. The first is the remove all the V pulses and the VDC connected.
3. The second is making all the Vdd and GND as the input ports. In place of all the symbols of the Vdd and GND make the input ports with the single name Vdd and GND.
4. After designing the schematic the go to LAUNCH→LAYOUT_XL. Then the layout window will open.
5. From the layout window goes to CONNECTIVITY→ GENERATE →All FROM SOURCE, we will get the input-output pins and the NMOS in the layout window then press SHIFT+F to get the layout of the pins and NMOS.
6. Enlarge the boundary of the layout by pressing S. Re-arrange the components inside the boundary.
7. To get the body terminal of the NMOS click on the NMOS and press Q then select BODYTYPE→DETACHED→OK.
8. Connect the output Y and the input S and the body terminal by using the metal wire. To obtain the wire press CTRL+SHIFT+X.
9. The other input G is connected using command VIA because the gate is a polysilicon.
10. To get the via CREATE→VIA. To get the polysilicon and the metal via go to the CLASS VIA DEFINITION→M1-POLY1.

11. The design of the layout is as shown in fig 9.

![Layout design of CS amplifier with resistive load](image)

**Figure 9**: Layout design of CS amplifier with resistive load

### III. Conclusion

Hence, the function of the common source amplifier with resistive load has been practically implemented by the cadence virtuoso tool and performs the ac, dc, transient analysis and layout of the common source amplifier with resistive load connected and output have been simulated.

### REFERENCES


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