Cell Structure and Power Analysis Using Dynamic Ram

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Abstract: The scaling of channels attains the current leakage at transistors, which shows the power lenience. In order to decrease the power and also to increase the speed of the structure, the size of the transistor is assumed to be low. Then it can also be changed. In this paper the dynamic RAM has been implemented for reducing the power. By analyzing the structure with 6T, N-CRAM in its features, a decreased power is reached, which is compared with the system in its active mode. The performance are analyzed in 1.8v which reduces the 90 percent of power than 6T, and 18 percent of power is reduced than in 8T cell, and 30 percent of current leakage is reduced in 6T cell. Thus it is compared to the existing SRAM, that leads to the cell with less power and storage of data is fine without distortion. So the constancy of the structure is increased when related to other cell. The result waveform gives that the cell contains improved stability and reduction in leakage using the cadence virtuoso of 180 nm technology.

Keywords: SRAM, RAM, DRAM

I. INTRODUCTION

The demand for low-power design and design trend is to increase the speed and working frequency of digital systems. Recently, some applications such as wireless sensor network, portable and battery-operated applications which involve SRAM as its major portion of its chip demand low power operation. As the MOSFETs are scaled down to nano-scale regime, statistical dopant fluctuations, oxide thickness variations and line edge roughness to increase the spread in transistor threshold voltage (Vth) and correspondingly affect the on and off currents. At sub-32nm channel lengths, achieving a large current drive while maintaining a low off-state leakage becomes difficult [1]. To solve this problem new technology MOSFET architectures involving the use of multiple gates controlling the transistor have been proposed. The FinFET device (is a self-aligned double-gate MOSFET) [1], CNTFET devices contain a straightforward process flow when starting from a conventional CMOS bulk transistor [4]. Steep sub threshold slope TFET, which utilizes the conduction mechanism in band-to-band tunneling, is one of the most promising candidates for ultra-low voltage/power applications. All these devices are used for the construction of the conventional 6T SRAM cell and its effect on various parameters are being studied in this paper[2].

The classical bulk-Si MOSFET structure down into the sub-20nm regime, SCE control requires heavy channel doping (>10^{18} cm^{-3}) and heavy super-halo implants to control sub-surface leakage currents [3]. As a result, carrier mobility’s are severely degraded due to impurity scattering and a high transverse electric field in the on-state. The off-state leakage current specification and on-state drive current is degraded. Off-state leakage current is enhanced in the band-to-band tunneling between the body and drain. Vth variability caused by random dopant fluctuations is another concern for nano-scale bulk-Si MOSFETs [3].

II. 6T SRAM CELL STRUCTURE

Static random access memory (SRAM) can retain its stored information as long as power is supplied [5]. This is in contrast to dynamic RAM (DRAM) where periodic refreshes are necessary or non-volatile memory where no power needs to be supplied for data retention, as for example flash memory. The term “random access” means that in an array of SRAM cells each cell can be read or written in any order, no matter which cell was last accessed. The structure of a 6 transistor SRAM cell, storing one bit of information, the core of the cell is formed by two CMOS inverters, where the output potential of each inverter V_{OUT} is fed as input into the other V_{IN}. This feedback loop stabilizes the inverters to their respective state. The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell [5]. In standby mode the word line is low, turning the access transistors off. In this state the inverters are in complementary state [7]. When the p-channel MOSFET of the left inverter is turned on, the potential V_{OUT} is high and the p-channel MOSFET of inverter two is turned off, V_{2OUT} is low[6].

To write information the data is imposed on the bit line and the inverse data on the inverse bit line, \(~\overline{BL}\). Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved [6]. For reading the word line is turned on to activate the access transistors while the information is sensed at the bit lines.
III. NC-SRAM CELL STRUCTURE

NC-SRAM cell is referred from the process of (dynamic) Active Voltage Scaling. This approach is used to decrease the excess of power, current and voltage. In the concept of NC SRAM cell as shown in Figure 2, N5 and N6 are the pass transistors which included with the conventional 6T cell module. That is presented with the change in ground voltages. This type of voltages are depends on modes of the cell. The transistor N5 is connected to positive source voltage and assigned to be active during sleep mode and the transistor N6 delivers the cell to be directly grounded during enable state. So these modes is analyzed by changing the voltage sources of the pass transistors and thus leakage is reduced. The positive voltage during sleep mode by N5, reduces the leakages at gate than by using N6, which grounds the cell. Thus for this method transistor pull down is raised when pass transistor is included which reduces the excess flow of current and voltage. Therefore the constancy for write is enhanced but read time is corrupted and the power intake is lessened. The transistors N5, N6 have high threshold voltages. Yet, the Transition time for read and write an operation is improved [9].

IV. 8T SRAM CELL STRUCTURE

A novel 8T SRAM cell structure to reduce the leakage current and dynamic power consumption has been reported in this work. The schematic of proposed 8T SRAM cell at 65nm technology is as shown in fig. 3. The proposed SRAM cell composed of write access transistor (M3), controlled by Write Word Line (WWL) and read access transistor (M8) is controlled by the Read Word Line (RWL). During the write operation WWL is transitions to high value and RWL and BLB both are maintained at Hence, the read access transistor (M8) cut OFF. To write „1“ into the cell Bit Line (BL) is pre charged to a high value, then „1“ is forced through the write access transistor (M3). Similarly, to write „0“ into the cell, BL is discharged. Hence, to perform write operation the proposed cell utilizing single BL, which could leads to reduction in the dynamic power consumption and leakage power [8].

During read operation, RWL is transition to high value and WWL is maintained at Hence the write access transistor is cut OFF. Prior to read operation BL and BLB are pre charged. Assume that „1“ is stored left and „0“ is stored right side, then BL discharged through M7 and M8. Since, „M6“ is cut OFF there is no path to discharge the BLB. Hence BLB is held at high value. Alternatively, if „1“ is stored right side, BLB is discharged through „M6“ and „M8“. Since, „M7“ is cut OFF there is no path exists to discharge the BL. Hence, it can maintain at high value. With this, storage nodes completely isolated from the Bit Lines (BL) during read operation, hence stability increases significantly.

V. DYNAMIC RAM

The structure is similar to 6T structure with transistors (NR1, NR2). These transistors are meant for reading. It is assumed as active by P2. N1 is for pulling down the bit. Whereas it represents the entire cell of (eight transistors); it is splitted as two cells. The structure has two circuits: read, write. The cell is consign to write like the 6T. The read performance is done by the transistors NR1,NR2. At idle, write mode, the transistors (NR1, NR2) is disconnected from the structure. By this method, the data stored in the structure leftover same till the next operation. This process is continuously repeats when (WRL becomes 0). Because (NR1 and NR2) transistors, the cell occupies moderate area, not higher than 10T. Due to this the array structure of the cell occupies more area for its location of memory when compared to 8T SRAM.

1.1 Principle
This SRAM requires 8T with dynamic RAM. Includes the supply is passed into the cell structure. The operation in sleep and write mode is analyzed by the cell and read is performed by WRL, BRL. Therefore during the sleep mode nodes are not initiated. The bit remains in structure. The WRL, BRL is initiated to read. Therefore, the data leftover in BRL. This is done with the data in B, which is assumed to be active with transistor P2. Same supply unit of vdd is passed to the read circuit. For the write mode the WL is initiated and the bit is transferred to the BLBAR to perform write 1 operation. The BL and BLBAR is charged. Therefore, the data leftover in BRL. This is done with the data in B, which is assumed to be active with transistor P2. Same supply unit of vdd is passed to the read circuit. For the write mode the WL is initiated and the bit is transferred to the BLBAR to perform write 1 operation. The BL and BLBAR is charged. Therefore, the data leftover in BRL. This is done with the data in B, which is assumed to be active with transistor P2. Same supply unit of vdd is passed to the read circuit.

1.2 Operation

Read process: The read cell WRL is high, and WL as low, so data is read and selected using P2 transistor. For 1 data read, the data stored in node A is 1, also mentioned as 0 bit write. N2 is not in active during in this mode. Consequently for logic 0 read, the data in A is low, and so that it is defined to be 1 data write. N2 is selected at this mode. Then BRL is selected to transfer the stored data to the cell.

Write process: while writing WRL as 0 and WL as 1. Hence the read cell is disconnected from the cell. The data in BL and BLBAR acts according to A.B. As in 6T write is performed by structure. Consequently, bit lines are preselected. While splitting the read, write cell the noise edge shows higher. The cell structure controls the inconstancy of the nodes. Single line (BRL) is considered for read process. So the bit lines (BL, BLBAR) are required for write. But the cell to write the data is lesser. So the power is reduced and also the power takes to read is 35% less and for write it takes 50% less when compared with 6T. But the area shows comparatively equal with 8T.

VI. SIMULATION RESULTS:

2.1 Transient analysis

The output performance of SRAM in write operation is analyzed in Figure 5. Therefore the consistent simulation for read and write is analyzed with the supply of 1.8v, technology with 180 nm. Where the performance of 6T is improved when analyzed with other SRAM. It takes less time to write the corresponding read bit while relating to other structure and it is around 6ps to 7 ps. Thus the corresponding bit is produced in the BL, when it remains in cell. Because of transistors (N5, N6) in NC structure, the bit takes more time than 6T but effective than 8T to reach in bit lines. It gives 4 % fall in NC, 2.5 % in 8T structure and 2% in dynamic RAM[10].

2.2 Power Consumption

Table 1 defines the power for the dynamic RAM in 180nm technology. The supply is 1.8v. The size of the structure is considered in constant value. The overall power is calculated. The power on leakage in 8T structure is 96% decreased with 6T cell, 19% greater with NC. The power reaches with 1.35 mw, which gives approximately equals to NC cell and lesser with existing systems. The power is analyzed by calculating the formula $P= \frac{1}{2} C V^2$. the same cell with 90 nm is compared that takes power as 118 µW with 1v supply in 6T with time 1.25u.

<table>
<thead>
<tr>
<th>TABLE:1</th>
<th>SRAM</th>
<th>6T</th>
<th>NC</th>
<th>8T</th>
<th>Dynamic RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER</td>
<td>42 µW</td>
<td>1 µW</td>
<td>1.5 µW</td>
<td>1.23 µW</td>
<td></td>
</tr>
</tbody>
</table>

2.3 DELAY

The Table 2 describes the delay, which defines the time that is taken by the bit to produce in BLBAR. The time consumption of 6T is faster than other SRAM structure. But NC, 8T is reduced by its speed because of additional transistors. In similar the dynamic RAM consumes lower power and a little delay, but lesser to 8T.

<table>
<thead>
<tr>
<th>Table:2</th>
<th>SRAM</th>
<th>6T</th>
<th>NC</th>
<th>8T</th>
<th>Dynamic RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>17.04 ps</td>
<td>25.02 ps</td>
<td>31.52 ps</td>
<td>30 ps</td>
<td></td>
</tr>
</tbody>
</table>

VII. CONCLUSION
The dynamic RAM is implemented, and the resultant power comparison is analyzed using cadence 180 nm technology. The supply used is 1.8v. By analyzing with 6T, and other SRAM cells the power savings are attained. The power tolerance is about 90% that is saved when analyzing with 6T. And 18% power is being saved in isolated read SRAM when related to 8T. Thus the dynamic RAM has achieved the reduced power and delay.

REFERENCES


Author’s Biographies

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